CLAIMS

What is claimed is:

1. A method of forming a transistor having a gate structure formed upon a substrate, comprising:

forming a first layer of nitride material over the gate structure and portions of the substrate adjacent the gate structure;

forming a layer of material having a relatively low dielectric constant over the first nitride layer;

patterning the low dielectric constant material to form low dielectric constant sidewall spacers adjacent the gate structure;

forming a second layer of nitride material over the first nitride layer and the low dielectric constant sidewall spacers;

patterning the first and second nitride layers so that the low dielectric constant sidewall spacers are encapsulated by nitride materials; and

doping portions of the substrate adjacent the gate structure to form source/drain regions therein, the sidewall spacers guiding dopant into select portions of the substrate.

2. The method of claim 1, further comprising forming a capping oxide layer over the gate structure prior to forming the first layer of nitride material, wherein the capping oxide layer underlies the first nitride layer.

3. The method of claim 2, further comprising:

forming source/drain extension regions within the substrate adjacent the gate structure prior to forming the first nitride layer.

4. The method of claim 3, further comprising forming one or more offset spacers adjacent the gate structure prior to forming the capping oxide layer, wherein the one or more thin offset spacers adjacent the gate structure substantially reduce overlap capacitance associated with the gate structure and the source/drain extension regions.

5. The method of claim 4, wherein the one or more thin offset spacers include at least one of an oxide spacer and a nitride spacer.

6. The method of claim 2, wherein the capping oxide layer mitigates loss of implanted dopants from the substrate up into overlying materials.

7. The method of claim 2, wherein implantation of dopants into the substrate to form the source/drain extension regions is substantially undeterred by the capping oxide layer.

8. The method of claim 1, wherein the low dielectric constant material has a dielectric constant of less than about 3.5.

9. The method of claim 1, wherein the low dielectric constant material includes at least one of black diamond from Applied Materials Inc., coral from Novellus Systems, Inc. and one or more low-k materials manufactured by JSR Microelectronics Corporation.

10. The method of claim 1, wherein at least one of the first nitride material, low dielectric constant material and second nitride material is formed to a thicknesses of between about 50 to about 500 Angstroms.

11. The method of claim 2, wherein the capping oxide layer is formed to a thicknesses of between about 50 to about 500 Angstroms.

12. The method of claim 1, further comprising:

patterning at least some of the first nitride layer in conjunction with patterning the layer of low dielectric constant material.

13. The method of claim 12, wherein an etching process utilized to pattern the capping oxide layer is selective relative to the nitride materials such that the sidewall spacers are substantially unaffected by an etchant utilized in the process, the sidewall spacers thus substantially retaining their respective shapes and remaining effective to guide dopants into desired locations within the substrate.

14. The method of claim 3, wherein at least one of the source/drain extension regions are formed to a depth of about 100-350 Angstroms, forming the source/drain extension regions comprises implanting a p-type dopant having a concentration of about 1E19 to 5E20 atoms/cm^3 to establish a PMOS transistor and forming the source/drain extension regions comprises implanting an n-type dopant having concentration of about 1E19 to 9.5E20 atoms/cm^3 to establish an NMOS transistor.

15. A transistor comprising:

a gate structure formed over a substrate;

sidewall spacers formed on the substrate adjacent the gate structure, the sidewall spacers including a low dielectric constant material encapsulated by one or more nitride materials; and

source/drain regions formed within the substrate adjacent the gate structure, the sidewall spacers serving to guide dopants implanted into the substrate to form the source/drain regions into desired locations within the substrate.

16. The transistor of claim 15, wherein at least one of the low dielectric constant material and the encapsulating nitride materials have a thickness of between about 50 to about 500 Angstroms.

17. The transistor of claim 15, wherein the low dielectric constant material has a dielectric constant of less than about 3.5.

18. The transistor of claim 15, wherein the low dielectric constant material includes at least one of black diamond from Applied Materials Inc., coral from Novellus Systems, Inc. and one or more low-k materials manufactured by the JSR Microelectronics Corporation.

19. The transistor of claim 15, further comprising:

a capping oxide layer formed over the gate structure, but under the sidewall spacers and encapsulating nitride materials, wherein an etching process utilized to pattern the capping oxide layer is selective relative to the nitride materials such that the sidewall spacers are substantially unaffected by an etchant utilized in the process, the sidewall spacers thus substantially retaining their respective shapes and remaining effective to guide dopants into desired locations within the substrate.

20. The transistor of claim 19, wherein the capping oxide layer mitigates loss of implanted dopants from the substrate up into overlying materials.

21. A method of forming a transistor having a gate structure formed upon a substrate, comprising:

forming a capping oxide layer over the gate structure and portions of the substrate adjacent the gate structure;

forming a layer of material having a relatively low dielectric constant over the capping oxide layer;

patterning the low dielectric constant material to form low dielectric constant sidewall spacers adjacent the gate structure;

forming a layer of nitride material over the capping oxide layer and the low dielectric constant sidewall spacers;

patterning the layer of nitride material so that the low dielectric constant sidewall spacers are encapsulated by nitride material; and

doping portions of the substrate adjacent the gate structure to form source/drain regions therein, the sidewall spacers guiding dopant into select portions of the substrate.

22. The method of claim 21, wherein the low dielectric constant material has a dielectric constant of less than about 3.5.